REMARKS

The Office Action mailed on June 26, 2006 has been received and its contents carefully considered.

The present Amendment revises claims 1, 12-15, and 20-22 to improve their form under U.S. claim-drafting practice and, where appropriate, to further distinguish the claimed invention from the prior art. Claims 7-10 and 28-31 have become redundant in view of other changes, so the present Amendment cancels them without waiver or prejudice. In addition, new claims 32-34 have been added to further protect the claimed invention. It is respectfully submitted that the pending claims 1-6, 12-19, 20-27, and 32-34 patently define over the prior art, as will be discussed below, and the rejections should be withdrawn in view of the revisions to the claims.

Regarding The Anticipation Rejection

Claims 7, 9, 12, 15-17, 20, 22, and 27 stand rejected under 35 U.S.C. §102(e) as anticipated by U.S. patent 6,216,224 to Klein. In view of the revisions to the claims, Applicants respectfully disagree. Furthermore, due to the claim cancellations described above, the rejection of cancelled claims 7 and 9 has been rendered moot.

Among the remaining claims being rejected for anticipation, claims 12 and 20 are independent. It is respectfully submitted that claims 12 and 20 are patentably distinguished from Klein for the reasons as below.

Claim 12, as amended, recites (with emphasis added):

> A method for accessing initialization data for starting up a central processor unit in a computer system that also includes a bus, a south-bridge chip connected to the bus, a non-volatile memory, and a north-bridge chip connected between the bus and the central processor unit, the method comprising:

(a) sending a request from the north-bridge chip to the south-bridge chip in order to access initialization data from the non-volatile memory, which stores a basic input/output system (BIOS) and the initialization data;

(b) in response to the request, accessing the non-volatile memory to read out the initialization data by the south-bridge chip;

(c) sending the initialization data from the south-bridge chip to the north-bridge chip; and

(d) upon receiving the initialization data sent from the south-bridge chip, activating the central processor unit for initialization based on the initialization data received by the north-bridge chip from the south-bridge chip.

It is respectfully submitted that claim 12, as amended, patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above.

The invention defined by claim 12 is directed to a method for accessing initialization data for starting a central processor unit in a computer system that includes a bus, a south-bridge chip connected to the bus, a non-volatile memory, and a north-bridge chip connected between the bus and the central processor unit in order to activate the central processor unit for initialization of the central processor unit based on initialization data received by the north-bridge chip from the south-bridge chip.

In rejecting claim 12, the Office Action relied on Klein, which focuses on read-only memory (ROM) shadowing. This is a process performed during booting of a computer system for transferring firmware routines from a ROM to a RAM before CPU initialization (see column 1, lines 13-44; column 2, lines 1-18; column 4, lines 7-17; column 4, lines 61-64). In particular, the Office Action relied on a few passages of Klein (e.g. lines 5-10 of column 1, lines 1-20 of

column 2, lines 55-57 of column 3) and Figure 1 showing the arrow from 104 to 116 (RAM) to reject the claim, where all cited passages relate to ROM shadowing.

However, ROM shadowing is a process for transferring firmware routines including routines of a BIOS from a ROM to a RAM before CPU initialization. This essential feature of ROM shadowing (that the firmware routines are transferred to and stored in the RAM) contrasts with claim 12, requiring "upon receiving the initialization data sent from the south-bridge, activating the central processor unit for initialization of the central processor unit based on the initialization data received by the north-bridge chip from the south-bridge chip." The marked contrast between ROM shadowing disclosure in Klein and the claimed invention, as in claim 12, will be more clear for the following discussion.

In contrast to claim 12, Klein in the "BACKGROUND OF THE INVENTION" section mentions (with emphasis added),

> FIG. 1 is a block diagram of the basic components of currently-available PCs that are involved in ROM shadowing. The firmware routines are stored as ROM data 102 in a ROM 104. During conventional ROM shadowing, the firmware routines are transferred, under control of the CPU 106, via an ISA bus 108, an ISA-20 PCI bus bridge 110, and a PCI bus 112 to a system controller 114. The system controller 114 then stores the data 116 in the RAM 118 via a memory bus 120. The CPU 106 repeatedly fetches and executes a small number of instructions from the ROM 104 via the ISA bus 108, the ISA-PCI bus bridge 110, the PCI bus 112, the system controller 114, and a CPU bus 122 in order to drive the system controller 114 to transfer the ROM data 102 to the RAM 118. When transfer of the firmware routines is complete, the CPU 106 is then initialized and, following initialization, the CPU fetches and executes the firmware initialization and BIOS routines directly from the system RAM 118 via the memory bus 120, system controller 114, and CPU bus 122. These routines direct the CPU 106 to read the operating system of the PC, or portions thereof, into the RAM 118 from a storage device (not shown), initialize various hardware and software system components (not shown), and

thereby bring the PC up to a state where it can be used by a human operator. (column 1, line 62 to column 2, line 18)

It is noted that during conventional ROM shadowing, the firmware routines (relied on by the Office Action as initialization data) are transferred, under control of the CPU 106, via an ISA bus 108, an ISA-PCI bus bridge 110 (relied on by the Office Action as south bridge), and a PCI bus 112 to a system controller 114. The system controller 114 (relied on by the Office Action as north bridge) then stores the data 116 in the RAM 118 via a memory bus 120. In contrast, claim 12 now requires, among other features, "(d) upon receiving the initialization data sent from the south-bridge chip, activating the central processor unit for initialization of the central processor unit based on the initialization data received by the north-bridge chip from the south-bridge chip" (emphasis added).

If Klein really anticipated claim 12, Klein would have disclosed or suggested that upon receiving the data of the firmware routines sent from the ISA-PCI bus bridge 110, the system controller 114 activated the CPU 106 for initialization of the CPU 106 based on the firmware routines received by the system controller 114 from the ISA-PCI bus bridge 110.

However, Klein does not teach this. Since Klein employs ROM shadowing, what Klein actually teaches is that upon receiving the data of the firmware routines that sent by the ISA-PCI bus bridge 110, the system controller 114 then stores the data 116 in the RAM 118 (see column 2, lines 1-3). In addition, regarding conventional ROM shadowing, the CPU 106 repeatedly fetches and executes a small number of instructions from the ROM 104 via the ISA bus 108, the ISA-PCI bus bridge 110, the PCI bus 112, the system controller 114, and a CPU bus 122 in order to drive the system controller 114 to transfer the ROM data 102 to the RAM 118 (see column 2, lines 6-18). Klein also discloses a method for ROM shadowing employing a ROM shadowing circuit in order to implement ROM shadowing, prior to the initialization of the CPU, as part of

the bootstrap process. When this ROM shadowing circuitry detects a system reset signal, the ROM shadowing circuit holds the CPU in a reset state while the ROM shadowing circuit drives the system controller to transfer the ROM data to the RAM. (column 3, lines 19-34)

Besides, Klein does not disclose that the system controller activates the CPU of Klein for initialization of the CPU upon receiving the ROM data 102 from the ISA-PCI bus bridge, even when the ROM shadowing is completed. Instead, reading the "ROM data" 102 from the RAM 118 via the system controller is essential for Klein. From the context of the cited paragraph above, Klein discloses that "**[w]hen transfer of the firmware routines is complete, the CPU 106 is then initialized** and, **following initialization**, the CPU fetches and executes **the firmware initialization and BIOS routines directly from the system RAM 118 via the memory bus 120, system controller 114, and CPU bus 122**" (column 2, lines 8-13, with emphasis added). Immediately, Klein sets forth that "**[t]hese routines direct the CPU 106 to read the operating system of the PC**, or portions thereof, **into the RAM 118** from a storage device (not shown), **initialize various hardware and software system components** (not shown), and thereby bring the PC up to a state where it can be used by a human operator" (column 2, lines 8-18, with emphasis added). Thus, it is clear that Klein discloses that the CPU 106 fetches and executes the "ROM data" 102 from the RAM 118 via the system controller 114 when the ROM shadowing is completed. This feature contrasts with what claim 12 requires in step (d).

From the context of Klein mentioned above, Klein discloses that the firmware routines, i.e. the "ROM data" 102 stored in the RAM 118, will not be fetched and executed by the CPU 106 of Klein until the CPU 106 of Klein is initialized. For example, Klein discloses that "[a]fter ROM shadowing is completed, the RSC 202 deasserts the CPU_RESET output signal, **allowing**

the CPU to be initialized and to begin executing firmware routines from the RAM 118" (see column 5, lines 4-8, with emphasis added). Klein discloses that firmware routines, i.e. the "ROM data" 102, from the RAM 118, are executed after the CPU is initialized**, but does not disclose any steps of CPU initialization**.

In contrast, claim 12 requires, among the other features, "(d) **upon receiving the initialization data that sent from the south-bridge chip, activating the central processor unit for initialization of the central processor unit based on the initialization data received by the north-bridge chip from the south-bridge chip**." Thus, Klein fails to disclose step (d) required by claim 12.

For at least the above reasons, it is respectfully submitted that claim 12 is not anticipated by Klein. Further, since Klein discloses a ROM shadowing method, Klein provides no suggestion or motivation to one of ordinary skill in the art at the time of the invention to change the principle of ROM shadowing in order to arrive at claim 12. Therefore, it is respectfully submitted that independent claims 12, as well as its dependent claims 15-17, is neither anticipated nor rendered obvious by Klein, and the rejection of these claims be withdrawn.

Independent claim 20, as amended, recites (with emphasis added):

> A system for accessing initialization data for starting a central processor unit, the system comprising:
>
> **a non-volatile memory storing a basic input/output system (BIOS) and initialization data**;
>
> **a south-bridge chip in direct communication with the non-volatile memory subsystem**, the south-bridge chip, when requested for the initialization data, **for accessing the initialization data from the non-volatile memory**;
>
> **a north-bridge chip, coupled between the south-bridge chip and the central processor unit, the north-bridge chip, when activated, sending a request for the initialization data to the south-bridge chip**;

wherein upon receiving the request from the north-bridge chip for obtaining the initialization data, the south-bridge chip accesses the initialization data and forwards the initialization data to the north-bridge chip for activating the central processor unit;

wherein **upon receiving the initialization data sent from the south-bridge chip, the north-bridge chip activates the central processor unit for initialization of the central processor unit based on the received initialization data.**

It is respectfully submit that claim 20, as amended, patently defines over the cited reference for at least the reason that the cited reference fails to disclose the features emphasized above.

The apparatus disclosed in claim 20 includes features similar to those required by claim 12. Consistent with the above discussion as to patentability of claim 12, claim 20 is neither anticipated nor rendered obvious by Klein. In particular, as above mentioned, during conventional ROM shadowing, the firmware routines (relied on by the Office Action as initialization data) are transferred, under control of the CPU 106, via an ISA bus 108, an ISA-PCI bus bridge 110 (relied on by the Office Action as a south bridge), and a PCI bus 112 to a system controller 114. The system controller 114 (relied on by the Office Action as a north bridge) then stores the data 116 in the RAM 118 via a memory bus 120. (See column 1, line 65 to column 2, line 3).

In contrast, Klein fails to disclose or suggest the north-bridge chip, as required by claim 20, wherein upon receiving the initialization data sent from the south-bridge chip, the north-bridge chip activates the central processor unit for initialization of the central processor unit based on the received initialization data. For at least the above reasons, it is respectfully submitted that claim 20, as well as its dependent claims 22 and 27, is neither anticipated nor rendered obvious by Klein. The rejection of claims 20, 22, and 27 should therefore be withdrawn.

Regarding The Obviousness Rejection

Claims 1-6, 8, 10, 13-14, 18-19, 21, 23-26, and 28-31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over applicants' admission of prior art and Klein. In view of the revisions to the claims, Applicants respectfully disagree. Due to the claim cancellations described above, the rejection of cancelled claims 8, 10, and 28-31 has been rendered moot.

Claim 1, from which claims 2-6 depend, now recites (with emphasis added):

> A method for accessing initialization data for starting up a central processor unit in a computer system comprising:
>
> (a) starting up a north-bridge chip that is coupled between the central processor unit and a south-bridge chip;
>
> (b) sending a request from said north-bridge chip to the south-bridge chip in order to access the initialization data from a non-volatile memory which stores a basic input/output system (BIOS) and the initialization data; and
>
> (c) upon receiving said initialization data from the south-bridge chip by said north-bridge chip, starting up the central processor unit for initialization of the central processor unit based on the received initialization data.

It is respectfully submitted that claim 12, as amended, patently defines over the cited prior art for at least the reason that the cited art fails to disclose the features emphasized above.

In rejecting claim 1, the Office Action asserts that the AAPA discloses claim 1 except "requesting initialization data from a south bridge chip." To resolve the deficiency of the AAPA, the Office Action asserts that Klein "teaches a system where BIOS and initialization data (102) is in a memory 104 connected to South Bridge 110 (Line 28 of column 4 mention that 110 is a PCI-ISA bridge, which is the South Bridge)" and "[t]he memory 104 connected to South Bridge 110

is storing both BIOS and initialization routines (lines 28-33 of column 1 mention that the firmware routines include BIOS and other initialization routines)."

Finally, the Office Action asserts that "[I]t would have been obvious to one [of] ordinary skill in the art to combine the teachings of Klein and applicant's admission of prior art" and "[o]ne [of] ordinary skill in the art would have been motivated to request initialization data of CPU from a South Bridge chip as disclosed in Klein, since it would make the system compact as only one shared non-volatile memory for BIOS and initialization data is required, which is accessed by CPU through South Bridge."

Applicants respectfully disagree with the assertions set forth by the Office Action for the following reasons.

In determining obviousness, it is impermissible to pick and choose from any one reference only so much as will support a given position, to the exclusion of other parts necessary to a full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

Firstly, the AAPA does not include "sending a request from said north-bridge chip to the south-bridge chip in order to access the initialization data from a non-volatile memory which stores a basic input/output system (BIOS) and the initialization data" and "upon receiving said initialization data from the south-bridge chip by said north-bridge chip, starting up the central processor unit for initialization of the central processor unit based on the received initialization data," as claim 1 requires. In contrast, the AAPA does require that "a serial PROM 200 is connected to the north bridge 204 by two input/output ports 202 of the north bridge 204" and "[a]fter the north bridge 204 has started up, it sends a clock-like signal to the serial PROM 200 and then reads the initialization data stored in the serial PROM 200." (See paragraph [0001] of the present application).

On the other hand, Klein discloses conventional ROM shadowing and a method for ROM shadowing. The two approaches are significantly different (see column 4, lines 26-46). Klein discloses conventional ROM shadowing that requires the CPU to repeatedly fetch and execute the code from the ROM for performing the ROM shadowing, and Klein also discloses a method for ROM shadowing that employs additional hardware, a ROM shadowing circuit (RSC), to drive the system controller to perform transfer of the firmware routines from a ROM to a RAM and the CPU is set to a reset state during the ROM shadowing However, Klein does not disclose or even suggest these features required by the claimed invention, as discussed above with respect to claims 12 and 20.

It is respectfully submitted that nothing in either the AAPA or Klein would suggest the modification proposed by the Office Action. The Office Action asserts that the motivation for the proposed modification to one of ordinary skill in the art is "since it would make the system compact as only one shared non-volatile memory for BIOS and initialization data is required, which is accessed by CPU through South Bridge". However, this reasoning for the proposed modification is a conclusory statement, not found in either the AAPA or Klein.

Moreover, one can question how the proposed modification is done and how it would result in the claimed invention. From the above discussion about the AAPA and the different ROM shadowing methods in Klein, one of ordinary skill in the art at the time of the invention would recognize that there is so much difference between the AAPA and Klein that the proposed modification would involve substantial redesign the AAPA and the booting process with ROM shadowing as in Klein. In view of this marked difference between the AAPA and the ROM shadowing processes employed by Klein, it is not at all clear just why one of ordinary skill in the art would have been motivated to modify the primary reference (i.e. the AAPA) basing on Klein, and how such a modification would result in the claimed invention.

Accordingly, it is respectfully submitted that since the cited references would not have provided a suggestion or motivation to one of ordinary skill in the art at the time of the invention to modify the AAPA in view of Klein so as to achieve the invention defined in claim 1, claim 1, as well as claims 2-6, is patentable over the cited references, and so the rejection be withdrawn.

Claims 13-14 and 18-19 depend from independent claim 12, as amended. Consistent with the above discussion, it is respectfully that claim 12 is neither anticipated nor rendered obvious by Klein. In rejecting claims 13-14 and 18-19 on page 11 of the Office Action, no suggestion or motivation is attributed to one of ordinary skill in the art at the time of the invention to modify or combine the AAPA with the ROM shadowing method of Klein so as to arrive at the claims at issue. For at least this reason, it is respectfully submitted that claims 13-14 and 18-19 patently define over the AAPA in view of Klein, and the rejection of these claims be withdrawn.

In particular, regarding claim 19 (which requires that "the initialization data includes serial initialization packet ("SIP") data"), the Office Action only sets forth that "lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs."

However, Klein discloses a method for ROM shadowing in a PC based on the Intel Pentium CPU (see column 4, lines 47-61; column 7, lines 8-22) and does not mention AMD CPUs. One of ordinary skill in the art would recognize that SIP data is for initializing AMD CPUs and a PC based on an AMD CPU differs from a PC based on the Intel Pentium CPU in at least the hardware and initialization operation between the CPU and the north-bridge. There is no suggestion or motivation to one of ordinary skill in the art at the time of the invention to combine or modify a ROM shadowing method employed in a PC based on the Intel Pentium

CPU and the transfer of SIP data for initializing AMD CPUs to arrive at the claimed invention. Therefore, it is respectfully submitted that the rejection of claim 19 should be withdrawn.

Claims 21 and 23-26 depend from independent claim 20 and are patentable along with it. Moreover, in rejecting claims 21, 23-26 on pages 11-12 of the Office Action, no suggestion or motivation is provided as to why one of ordinary skill in the art at the time of the invention would modify or combine the AAPA with the ROM shadowing method of Klein to arrive at the claims at issue. For at least this reason, it is respectfully submitted that claims 21, 23-26 patently define over the AAPA in view of Klein, and the rejection of these claims be withdrawn.

Regarding claims 18 and 23, the Office Action asserts that "Klein mentions that the address counter preloads an initial address, which is the highest address for ROM data that is transferred from ROM to RAM in lines 30-35 of column 5" and "[t]hus, ROM data contains an initialization ID." Applicants respectfully disagree. The initial address of Klein, relied on by the Office Action, is used for a ROM shadowing circuit (RSC) to perform transfer of firmware routines from a ROM to a RAM (see column 5, lines 14-31), not for initialization of the CPU. For at least the above reason, Klein does not disclose initialization data. It is respectfully submitted that the rejection of claims 18, 23, and 30 should be withdrawn.

New claims 32-34 have been added to further protect the claimed subject matter regarding independent claims 1, 12, and 20, respectively. It is respectfully submitted that the cited references do not disclose or suggest "upon receiving said initialization data from the south-bridge chip by said north-bridge chip, starting up the central processor unit to set initial values for initialization of the central processor unit based on the received initialization data," as required by claim 32. Similar features are also found in claims 33 and 34. It is submitted that claims 32-34 define over the cited references.

Conclusion

Based on the foregoing, it is submitted that this application is in condition for allowance. Notice of such action and the passing of this case to issue are therefore respectfully requested.

Respectfully submitted,

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